

ABSTRACT OF THE DISCLOSURE

There is provided a boosting circuit in which a boosting efficiency is enhanced without increasing a chip area, and a time required for reaching a desired boosting voltage different in a voltage level and current ability is shortened. A stage-number switching circuit (20), for switching an output terminal of a charge pump circuit (12) and an input terminal of a charge pump circuit (13) between a connected state and an unconnected state, enables clock signals (CLK1, CLK3) to be supplied to the charge pump circuit (11) among 4-phase clock signals (CLK1 to CLK4) to be supplied to 2-stage charge pump circuits in the case where a stage-number switching control signal (SWHON) is at a supply voltage VDD level, is synchronized with pumping of the charge pump circuits, and turns on an internal switching transistor at a potential higher than a boosting potential of the charge pump circuit (12) in the previous stage, whereby the 2-stage charge pump circuits (11, 12) and the 2-stage charge pump circuits (13, 14) are connected in series with each other.